



The cover features a large, stylized title 'TOWARDS HARDWARE REJUVENATION' in a serif font. The word 'TOWARDS' is written vertically to the left of 'HARDWARE'. The background is a light gray with a faint, circular watermark of a university seal on the left side. The seal contains the text 'Faculdade de Engenharia' at the top, 'Ciência e Tecnologia' on the sides, and 'Comitê de' at the bottom. The right side of the cover has a vertical bar with three colored segments: dark brown, light brown, and dark brown.

TOWARDS **HARDWARE**
REJUVENATION

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Reconfigurable Hardware

- High performance
- High flexibility
- Increasingly being used in production
- More prone to faults

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Field Programmable Gate Arrays [FPGA]

- Technologies
 - Radiation hardened and anti-fuse
 - SRAM-based
- System design
 - Development in VHDL, Verilog or SystemC
 - Hardware definition file (*bitstream*)
 - Loaded to the FPGA SRAM during boot up
 - Dynamic Partial Reconfiguration

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Hardware Faults

- Permanent faults
 - Irreversible physical changes
- Transient faults
 - Cosmic radiation and electromagnetic interference
 - Operating environment
- Intermittent faults
 - Unstable hardware
 - Activation depends on environmental conditions

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Reprogrammable HW Aging

“The progressive loss of functionality, performance degradation or malfunction due to the accumulation of failures in programmable logic cells”

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Reprogrammable HW Rejuvenation

“The proactive *refreshing* of the internal logic of the running device, to prevent failures in the future.”

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Available Technologies

- **Scrubbing**
Reload the configuration memory with the original *bitstream*
- **Relocation**
Relocate the design to a different configuration memory location
- **Redundancy**
Reuse spare cells to implement spatial redundancy

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Research Questions

- What are the effects of HW aging in FPGAs?
- What is the best strategy for deciding the refreshing instant?
- What should be refreshed?
- What level of redundancy will be necessary?
- How to deal with running applications?

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